REMARKS

Applicants received a Final Office Action mailed from the Patent Office on October 8, 2002. Claims 1-26 and 30 stand rejected as being anticipated by *Tanaka et al.* (US Patent 5,559,737), hereinafter "*Tanaka*". Applicants submit these remarks in response to the Final Office Action.

The Final Office Action rejected claims 1-26 and 30 as being anticipated by *Tanaka*. However, the Final Office Action only points to the figures of *Tanaka* for evidence that the claimed invention is anticipated. The figures of *Tanaka* invariably show that multiple transistors equalizing the two circuits at multiple points are used to produce the desired equalizing effect. The Applicants have claimed use of only a single transistor for equalization purposes, thus improving upon the design illustrated by *Tanaka*. If anything, by consistently illustrating equalization of the two circuits in multiple places with multiple transistors, *Tanaka* teaches away from the claimed invention and illustrates a more complex design requiring a two-polarity signal generator and other additional circuitry. The Final Office Action indicates that *Tanaka* uses a single transistor for equalization and uses the other transistors for equalization of other portions of the circuitry. However, Applicants clearly claim a circuit that uses a single transistor for equalization of all of the circuitry in question, and thus cannot be said to be encompassing the circuit of *Tanaka* within the claims.

As stated in the Abstract, *Tanaka* equalizes the potential between a cell and a dummy cell at two points: 1) between a bit line and a dummy cell bit line and 2) between a sense line and a dummy cell sense line. The gate nodes of two different equalizing N-channel transistors are coupled to a pulse generator as shown in Fig. 2, Fig. 5, and Fig.

11. The first and second nodes of the first equalizing transistor are coupled to the bit line and the dummy cell bit line respectively as also shown in Fig. 2, Fig. 5, and Fig. 11. The first and second nodes of the second equalizing transistor are coupled to the first and second nodes of an equalizing P-channel transistor and to the sense line and the dummy cell sense line respectively. (*Tanaka*, Fig. 2, Fig. 5, and Fig. 11). The gate node of the equalizing P-channel transistor is coupled to a complementary output pulse from the pulse generator. (*Tanaka*, Fig. 2, Fig. 5, and Fig. 11). Thus, *Tanaka* utilizes 3 equalizing transistors and a pulse generator to generate both a pulse and its complement; whereas, the presently claimed invention utilizes a single equalizing transistor to provide similar performance characteristics as shown by comparing Figures 4A-4B of the present invention and Figures 3, 6, and 12 of *Tanaka*. As a result, the presently claimed invention makes the cited art of *Tanaka* simpler without loss of capability. The independent claims 1, 12, 16, 20, 24, and 30 of the present invention have been amended to include a single equalizing transistor. This important development results in significant savings both in the expense of manufacturing the memory device and in the size of the device.

As amended, claims 1, 12, 16, 20, 24, and 30 include an element not found in the cited art. Thus, these claims are ready for allowance. Because all of the remaining claims depend on the now allowable independent claims 1, 12, 16, 20, 24, and 30, these claims also stand ready for allowance.

Condition for Allowance

Applicants submit that all rejections have been overcome and the present application is now in condition for allowance. If the Examiner has any questions or comments, the Applicants respectfully request that the Examiner contact the undersigned by telephone.

Deposit Account Authorization and Extension of Time Request

Please charge any shortages and credit any overages to Deposit Account No. 02-2666, including any funds necessitated due to insufficient funds for an accompanying check. Any necessary extension of time for response not already requested is hereby requested. Please charge any corresponding fee to Deposit Account No. 02-2666.

Respectfully submitted,

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